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Compound Adder Design Using Carry-Look-ahead / Carry Select Adders

Jayaprakash M [(1)] A. Shanmugam [(2)]

[(1)] Assistant Professor, Department of Electronics and Communication Engineering, SCAD Institute of Technology, Coimbatore, Tamil Nadu, India.
[(2)] Principal, Bannari Amman Institute of Technology, Sathyamangalam, Tamil Nadu, India.

Abstract
To reduce fan-out load at the final multiplexor stage and to relieve the speed requirement of compound adders, a parallel global carry generation is used for a hybrid carry-look ahead/ carry-select adder design. To develop the speed and to minimize silicon area, a new logical decomposition is derived. The new architecture has been explained with a 64-bit adder design using dynamic CMOS circuit implementations. The 64-bit adder has the delay of 525ps in 0.225µm bulk CMOS technology

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Carry look ahead adder, Carry select adder, CMOS, Fan-out, Multiplexor

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