Manuscript ID : 00000-66722

Source ID : 00000089

International Journal of Research in Electronics & Communication Technology

Volume 1, Issue 1, July-September 2013, Pages 72-77, Page Count - 6

FPGA Implementation of 32 point Radix-2 Pipelined FFT

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Abstract

This paper presents an advanced method of implementing Fast Fourier Transform(FFT) using pipelining concepts. FFT is a technique which efficiently calculates the DFT by reducing the number of addition and multiplication operations taken place. In this paper ,in between the intermediate stages of every butterfly, pipelining is used to store the outputs of previous stages. Then, the development of 32-point FFT based on Decimation-In-Time radix-2 algorithm has been done. Pipelining is used to enhance the speed by decreasing the clock period and hence to improve the throughput of the FFT processor.

Author Keywords

Fast Fourier Transform, Decimation In Time, Pipelining, Radix-2, Registers

ISSN Print: 2348-0017
ISSN Online: 2347-6109
Source Type: Journals
Document Type: Journal Article
Publication Language: English
DOI:
Abbreviated Journal Title: IJRECT
Access Type: Open Access
Publisher Name: IAEME Publication
Resource Licence: CC BY-NC
Major Subject: Physical Sciences
Subject Area classification: Engineering and Technology
Subject area: Electronics Engineering
Source: SCOPEDATABASE

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